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RECYCLING OF PRINTED CIRCUIT BOARD BY TEMPERATURE SHOCK

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ABSTRACT
In this contribution we are dealing with the possibility of electronic waste separation by temperature effect. It gives a possible direction how to solve the problem of increasing with electronic waste not only in Czech Republic, but also throughout the world. Further, we are dealing with of heat transfer inside the printed circuit boards (PCB) and with thermal longitudinal expansion of used material in the FEMLAB software environment. The problem is modelled also in other programs, which offer the view of the whole structure of used materials and subsequently their movement in dependence on the changes of the ambient temperature. With the use of the utilize experience from detail references background research and various software simulators we achieved the maximum analysis of the problem. The solving, which resulted from the calculations of shear stress of given materials was subsequently verified in laboratory. The development of new criteria for PCB recycling has opened new possibilities of treatment for used materials.
Keywords: Electronic waste, printed circuit boards (PCB), recycling, separation, heat transfer, shear stress

1. INTRODUCTION
In the last twenty years the problem of material recycling, especially the electronic waste has been focused on by specialists of electronics. The production and subsequent consumption parts is generally growing and after termination of their time life usually end up on dumps solid and for hazardous waste, because these products contain also the materials, which represent potential risk the for environment as well as for human health. For this reason we have to look for any possibility of recycling these materials.

2. THEORY
A printed circuit board is the essential part of the assembling technology of all electronic wholes. Is serves as supporting element of parts, it has mechanical function, interlock it provides the lost heat exhaustion, functions as an electric and recently also as an optical connecting member between parts and systems [1].

2.1. PCB materials
For surface assembly the PCB material should have approximately the same coefficient of linear expansion as the material of the used parts. For reason of different of heat dilatation PCB and parts, was growing the mechanical stress of soldered joint. But at the same time, the magnitude of mechanical stress is given by the difference of the linear expansion coefficients. According to previous experiences, in common application of surface mount assembly on a glass-epoxide PCB

(FR4) it is possible (with no risk of subsequent cracking of soldered joints) to mount miniature passive parts (resistors, ceramic capacitors) of the size up to 10 mm, integrated circuits in SO version, plastic microchip carriers, flat pack and quad pack circuits, TAB (Micropack) etc.

2.2. Thermal stress in two-layer plate exposed by the temperature changes

Particular layers generally have each different values of mechanical characteristics, especially of Young modulus and thermal expansivity . In case of thermal change, the layers prevent each other from rising of their own thermal dilatations which correspond to the temperature change. Let´s expose two-layer wall to the temperature change from starting (referential) status which is supposed to be without the stress. If the both layers were separated from each other, the relative length change each of them

$$\varepsilon_k^T = \alpha_k \Delta T \quad , \quad k = 1,2 \quad , \quad \Delta T = T - T_m \quad ,$$

would be identical in all directions, in case that isotropy is supposed to be characteristic for the both layers. As it is shown in the fig. 1, the difference between thermal dilatation of layers is balanced by their elastic deformation. By warming or cooling in ΔT embodies the wall outside (membrane deformations is not prevented) certain macroscopic – efective length change ε^T. Let´s imagine (without a detriment to the task commonness) that ΔT is plus, i. e. warming, and $\alpha 2 > \alpha 1$. The layer 2 (plastic material) is then compressed, the layer 1 (Cu – conductive way) is spreaded – see fig. 1. Membrane deformations of the plate are free, so that membrane forces in cuts of the wall are neutral. Holds so:

$$n_i = \sum_{k=1}^{2} s_k \sigma_{ki}^T = 0 \quad , \quad i = x, z. \tag{1}$$

The stress state in each layer is unibiaxial, so we can leave out then index *i*. The deformation in the both layers are equated to ε^T and given by algebraic sum of thermal dilatation and elastic deformation, i. e. holds

$$\varepsilon^T = \varepsilon_k + \varepsilon_k^T . \tag{2}$$

Equation of elasticity for k-th layer can be written at this form

$$\varepsilon_k = \frac{1}{E_k}\left(\sigma_k^T - \nu_k \sigma_k^T\right) = \frac{\sigma_k^T}{E_k^*} . \tag{3}$$

After substitution (3) into (2) is

$$\varepsilon^T = \frac{\sigma_k^T}{E_k^*} + \alpha_k \Delta T . \tag{4}$$

If we express σ_k^T from here and substitute into equation of balance (1), we will get for the effective dilatation of the wall

$$\varepsilon^T = \frac{\sum_{k=1}^{2} E_k^* s_k \alpha_k}{\sum_{k=1}^{2} E_k^* s_k} \Delta T = \alpha \Delta T \tag{5}$$

Thermal tensity values are then

$$\sigma_k^T = E_k^* \Delta T \left(\alpha - \alpha_k\right) \quad , \quad k = 1,2. \tag{6}$$

Above-mentioned relations for thermal stress don´t stand in the places of free edges, where is necessary to solve the appropriate edge problem. Let´s imagine that layers are totally separated from each other in the whole surface and consistency of layers ensure thoughtfully only plugs putting at the edge of the plate. It is evident that resultant of the thermal tensity in the both layers strain thought plugs at cutting. The function of plugs ensure adhesive layer connection. By the edge of the board rise shear stress tips at the boundary line of layers – see fig. 2. If their values reach up to

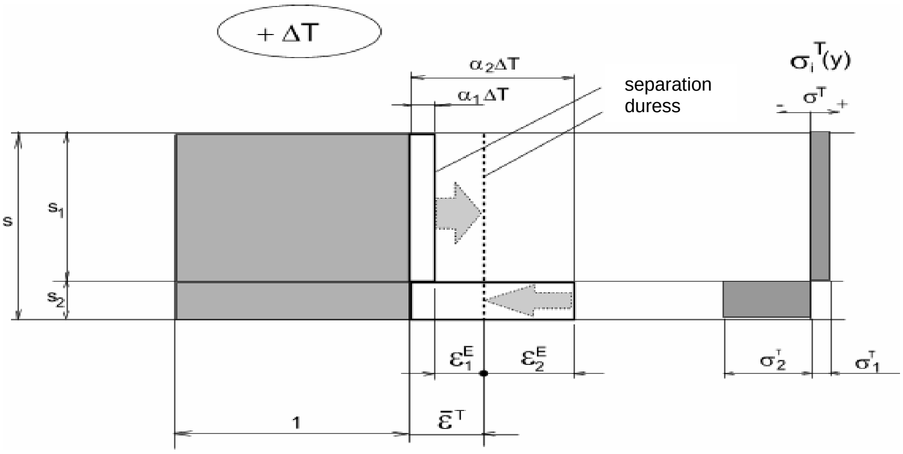

Figure 1. Thermal-mechanical behaviour in two-layer wall

shear strength limit of adhesive layer connections, separations will rise at the edge of two-layer wall that are extending far from the edge of a plate.

Modelling of two-layer board thermal tensity

Above-mentioned consideration can be generalize at cases of incidence of general-transiental thermal fields. FEM modelling of appropriate status of transient thermal stress comes through two phases. In the first phase are entered appropriate thermal boundary conditions of the plate and at specific time steps will be figured out the relevant thermal field profiles. In the second phase are entered appropriate mechanical boundary conditions and for specific time shots of temperature process in the plate will be figured out the appropriate immediate stress status – value of components of transient thermal stress at the given time moment. Temporally variable thermal boundary conditions are entered through so-called time curves. While mechanical and thermal characteristics of layer material 1 (Cu) can be considered in calculation as thermal independent, polymeric layer 2 shows expressive temperature dependences of physical property, especially of elasticity module. In calculations these dependences were take into account by appropriate thermal curves.

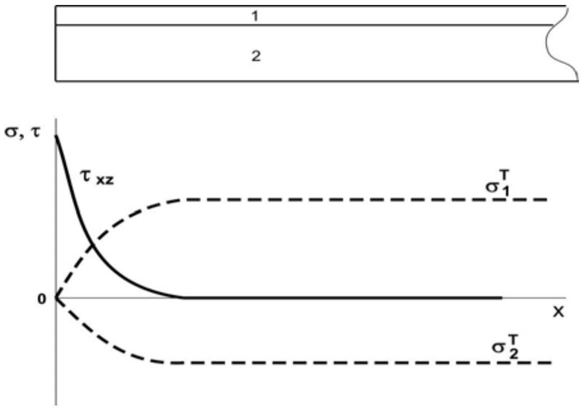

Figure 2. Thermal stress character by temperation warming of two-layer wall at its free edge

In the fig. 3 temperature process on two-layer board thickness Cu/EP by thermal shock is illustrated. The board heated at 250°C is put into brine of temperature –15°C. The temperature process corresponds to 5 sec period from the moment of submersion. The appropriate shear stress process at the edge of the plate in the interface of the layers round free board edge is shown in the figure.

2.4. Computer simulation of PCB heating

In this chapter we deal with the heat transfer in PCB. It is important to know the time, in which the whole PCB heats up to the required temperature. To solve this problem we used the FEMLAB software. The ground is the creation of the required model with boundary conditions and properties of the used materials. The behaviour of individual simulations for given times are shown in the following figure.

3. CONCLUSION

We have worked out a study of PCB production, because it is necessary to know the manufacturing process to able to find the ways of recycling. We followed the PCB production from the beginning to the phase when it is ready for the market.

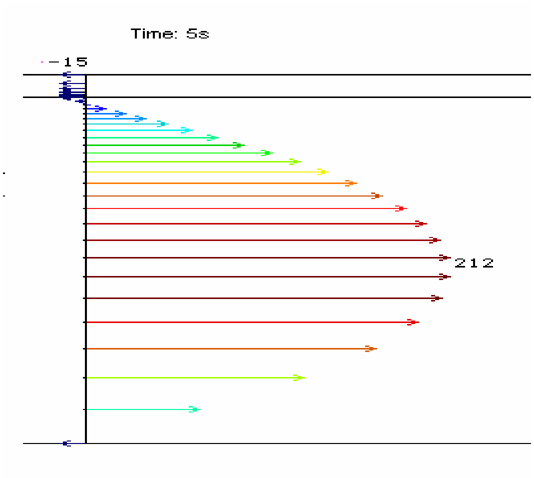

Figure 3. Temperature profile on two-layer wall

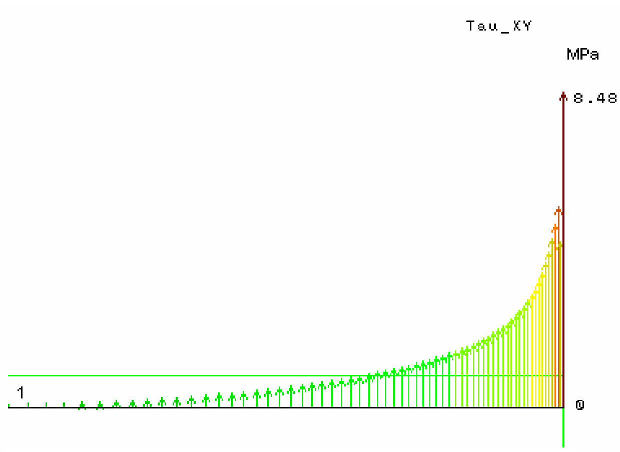

Figure 4. Interface stress state at the edge thickness by thermal shock for time of 5 sec of a two-layer plate

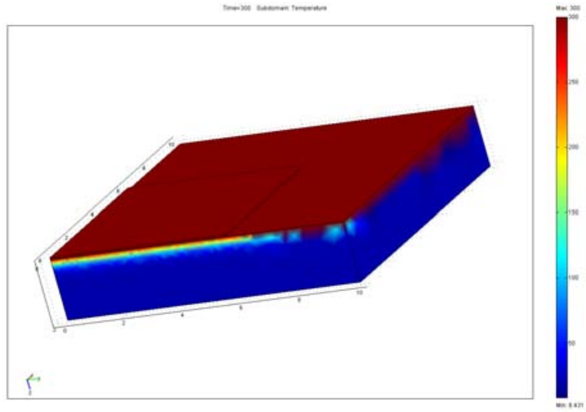

Figure 5. Heating of the epoxide resin board during 300s up to the temperature of 300°C

Figure 6. The laboratory separation of the conductive ways by temperature shock

Further, we calculated the shear stress, which is needed to separation conductive copper ways from epoxide resin. We used several ways of PCB heating-up, for example heating-up the board in tempered press up to the temperature of 200°C. After, it was cooled in brine. Heating-up to 350°C by a proved to be the best approach. This temperature is sufficient also for the separation of tin, which the parts are soldered with the melting point of tin is 250°C. After using the mechanical separation, the fell off the PCB. We used the mechanical separation also to remove the conductive ways (See Fig.5). This case shows a resemblance with adhesive joints theory. However, laboratory test showed that the temperature difference must be much higher than shown in the calculation. It results from the fact that copper is very plastic and the calculated dilatation caused by the temperature difference is smaller. This way of recycling could lead to a possible industrial application and thereby to contribute to environment protection.

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5. ACKNOWLEDGEMENT

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