17th International Research/Expert Conference
"Trends in the Development of Machinery and Associated Technology"
TMT 2013, Istanbul, Turkey, 10-11 September 2013

DESIGN OF AN INTEGRATED PLANAR INDUCTOR USING 0.35 μM FABRICATION TECHNOLOGY

Sabrije Osmanaj
University of Prishtina, Faculty of Electrical and Computer Engineering
Pristine, Kosovo
sosmanaj@gmail.com

Erdet Nasufi
University of Prishtina, Faculty of Electrical and Computer Engineering
Pristine, Kosovo
erdet.nasufi@gmail.com

ABSTRACT
In this paper, is presented and analyzed physical model of integrated planar inductor for 0.35 μm fabrication technology. According to CMP, C35B3C0 fabrication technology provides three metallic layers; therefore, there is no need to use poly-silicon or diffused underpasses. The metalic-1 layer is used for underpasses. Operation voltage of IC's fabricated with this technology is 2.5 to 3.6 V. The physical model of the integrated planar inductor is designed using "The Electric VLSI Design". The purpose of this paper is to present and compare the results of total inductivity of inductors with different number of turns. Grover's expressions are used for calculations. Simulated results for parasitic and resistance capacities for our model are presented in this paper, too.
Keywords: *CMOS proces, planar inductor*

1. INTRODUCTION
Inductors have a substantial importance on cell circuits such as: oscillators, filters, signal amplifiers, power amplifiers, low-noise amplifiers, etc. As those cells constitute highly integrated RF and analog circuits, then need to design very-large-scale integrated inductors is increased [1]. Designing very-large-scaled integrated inductors is more challenging than other passive components.
There are several different integrated inductors layouts. The rectangular spiral, hexagonal spiral and circular spiral respectively are mostly used layouts [2]. The spiral planar inductor can be fabricated only by using two or more metallic layers fabrication processes, because one of layers is used for underpass. In this paper, rectangular spiral layout is used to design four winding planar inductor.

2. FABRICATION PROCESS
Fabrication process is based on 1P3m standard – one polysilic layer (1P) and three metallic layers (3M). According to X-FAB [4] fabrication process datasheet, thickness of metallic layer number 2 and number 3 is 1 μm, whereas thickness of metallic layer number 1 is 0,58 μm. Sheet resistance of first metallic layer is 0,090 Ω, and the sheet resistance of second and third metallic layers is 0,045 Ω. Capacitance for micrometer square of isolated layer between metal-2 and metal-3 is 1,25 fF/μm^2, whereas perimeter capacitance is 0,111 fF/μm. According to design roles [4], minimal width of metallic layer Metal-1, Via-1 and Via-2 is 0,5 μm, and distance between conductive traces is 0,45 μm. Width of the conductive traces on layers Metal-2 and Metal-3 is 0,6 μm, and distance between these

traces is 0,5/0,6 µm. XU035 [4], offers extra power conductive connections, where width of these conductive connections is 3,0 µm and distance between them is 2,5 µm.

3. DESIGN OF PLANAR INDUCTOR

Figure 2 shows top view of planar inductor. Four windings rectangular spiral layout is used for this design [3]. As shown, distance between turns is 1µm, and width of conductive traces is 1 µm. These sizing parameters are consistent with design rules listed on datasheet [4]. Turns are layout on third (upper) metallic layer. Middle (second) metallic layer is used for underpass – connecting the end of inner turn with node number 2. As shown in figure 2, metallic traces layout on second metallic layer is of 9 µm length. Total size of this inductive coil is 23 µm x 18 µm. Figure 1 shows three-dimension view of the planar inductive coil.

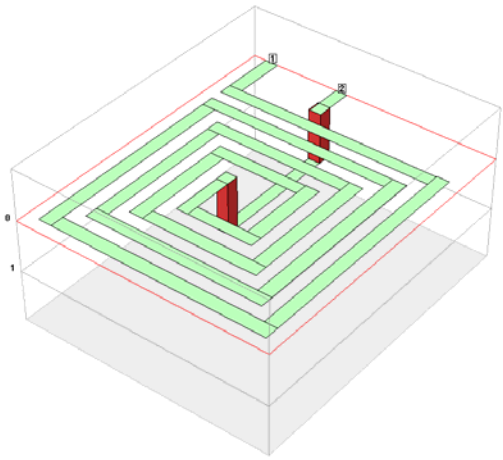

Figure 1. 3D view of rectangular planar inductor.

4. CALCULATION OF SERIES RESISTANCE

For uniformly distributed direct current on rectangular cross-section view conductor, with length L, resistivity ρ, resistance is given by:

$$R_{DC} = \rho \frac{L}{Wt} \quad \text{..... (1)}$$

As resistance of metallic layers are expressed in terms of sheet resistance on datasheet [4], then resistance calculation is given by:

$$R_{DC} = R_S \frac{L}{W} \quad \text{.....(2)}$$

Calculated resistance is valid for direct currents and low frequency currents. At increasing frequencies, the current density becomes more and more nonuniform due to high frequency effekt in metalls [4]. Resistance of rectangular cross-section conductors on high frequencies, based on direct-current resistance is given by (3):

$$R_{AC} = R_{DC}\left[1 + \left(\frac{f}{f_l}\right)^2 + \left(\frac{f}{f_u}\right)^2\right]^{\frac{1}{10}} \quad \text{.....(3)}$$

$$f_l = \frac{\pi\rho}{2\mu_r\mu_0 Wt} = \frac{\pi R_S}{2\mu_r\mu_0 W} \quad \text{.....(4)}$$

$$f_u = \frac{\pi^2 R_S}{\mu_r\mu_0}\left[K\sqrt{1 - \frac{t^2}{W^2}}\right]^{-2} \quad \text{.....(5)}$$

where W and t are dimensions of rectangular conductur cross-section, μ is magnetic permeability (μ_r is taken 1), f_l and f_u are low and high cut-off frequencies, and K is first order elliptic integral and is given by

$$K(x) = \int_0^{\pi/2} \frac{1}{\sqrt{1 - x^2\sin^2\varphi}} d\varphi, \text{ ose } K(x) = \int_0^1 \frac{1}{\sqrt{(1-t^2)(1-xt^2)}} dt \quad \text{.....(6)}$$

Taking $W = 1\ [\mu m]$, $t = 1[\mu m]$, $R_S = 0.045$, $\mu_r = 1.00$ and $x = [0;\ 0.2;\ 0.4;\ 0.6;\ 0.8]$, low cut-off frequency is $f_l = 5.62\ GHz$, and high cut-off frequency for different values of K parameter are listed on table 1. Resistance of coil on high frequencies – from 0.5 GHz to 10 GHz – for different values of K parameter are calculate and are shown in figure 2.

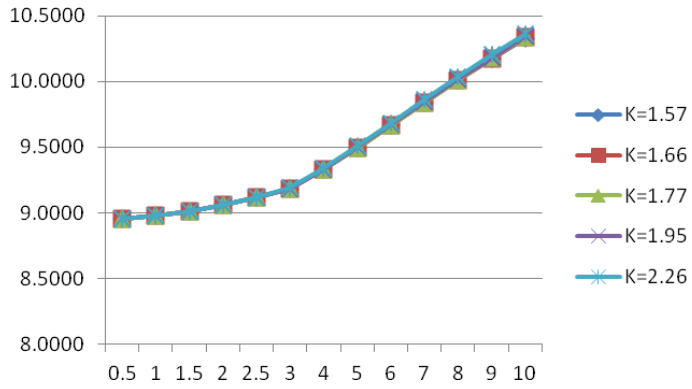

Figure 2. Calculated resistance depending on the frequency for different values of K parameter.

4.1. Self-inductance calculations

Self-inductance for a straight conductor according to Grover's equations extracted from (5), is

$$L = 0.002l\left\{ln\left|\frac{2l}{GMD}\right| - 1.25 + \frac{AMD}{l} + \frac{\mu T}{4}\right\} \quad ...(7)$$

where L is self-inductance [μH], l is length of conductor [cm], and GMD and AMD are geometric and arithmetic mean distance of cross-sections, respectively, μ is magnetic permeability of conductor, and T is frequency-correction parameter.

The mutual-inductance between two parallel conductors is a function of the length of the conductors and of the geometric mean distance. In general,

$$M = 0.2lQ \quad ...(8)$$

where M is the mutual-inductance in nH, l is the length of conductor in mm, and Q is the mutual-inductance parameter, calculated from the equation

$$Q = ln\left\{\frac{l}{GMD} + \sqrt{1 + \frac{l^2}{GMD^2}}\right\} - \sqrt{1 + \frac{GMD^2}{l^2}} + \frac{GMD}{l} \quad ...(9)$$

$$GMD = d \cdot \exp\left[-\left(\frac{w^2}{12d^2} + \frac{w^4}{60d^4} + \frac{w^6}{168d^6} + \frac{w^8}{360d^8} + \frac{w^{10}}{660d^{10}}\right)\right] \quad ...(10)$$

where w is the track width and d is distance between track centres (5). Whereas, according to (5), mutual-inductance of two different length traces, in case of $p = q$ is

$$M_{j,m} = M_{m+p} - M_p \quad ...(11)$$

and in case of $p = 0$ is

$$2M_{j,m} = (M_j + M_m) - M_q \quad ...(12)$$

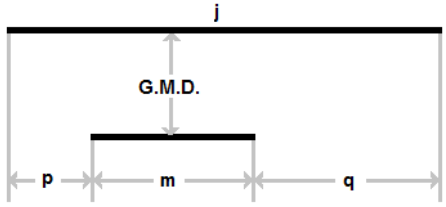

Figure 3. Two different length parallel conductors.

General expression of total inductance of inductor is given by $L_T = L_0 + \sum M$, where L_T is the total inductance, L_0 is the total self-inductance, and $\sum M$ is total mutual-inductance. In case of parallel conductors where current flows in positive direction and the others where current flows in negative direction, the total inductance is expressed by $L_T = L_0 + M_+ - M_-$, where M_+ is the total positive mutual-inductance, and M_- is total negative mutual-inductance. Calculated total inductance value of designed inductor is 12,0745 nH. As noticed, total mutual-inductance has no any large effect on

calculated total self-inductance. Resulting S-parameters of 0.1 GHz up to 10 GHz frequency range are shown in figure 4.

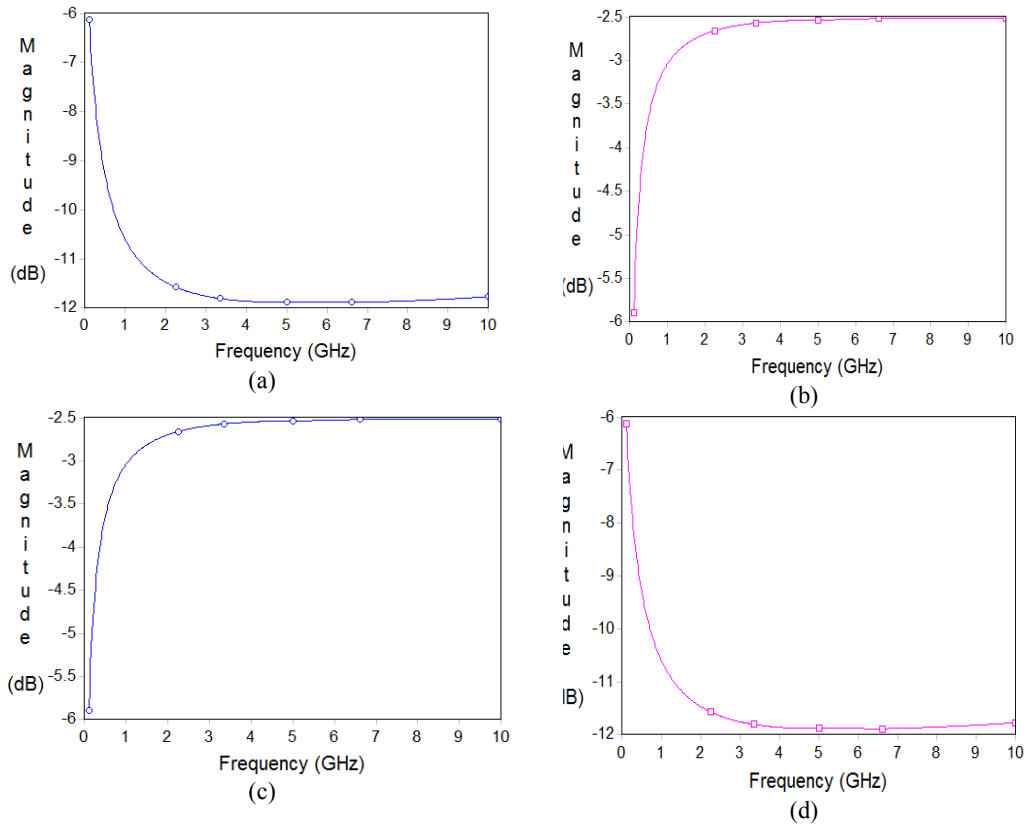

Figure 4. S-parameters of inductor on frequency range 0.1 GHz – 10 GHz.
(a) the port-1 voltage reflection coefficient, S_{11}; (b) the reverse voltage gain, S_{12}; (c) the forward voltage gain, S_{21}; (d) the output port voltage reflection coefficient, S_{22}.

5. CONCLUSIONS

In this paper, design, size and calculations results are represented for rectangular planar inductor. Size of the four windings planar inductor is 23 µmx18 µm. This inductor is characterized by 8,59 Ω direct-current resistance and it's increased by increasing the frequency. This is caused by skin-effect. Total calculated inductance of the designed planar inductor is 12,0745 *nH*, which is not very high value, but as this is a very-large-scale integrated inductor, wiring a series of such inductors is possible to gain higher total inductance value.

6. REFERENCES

[1] J. Aguilera, R. Berenguer, "Design and Test of Integrated Inductors for RF Applications", Kluwer Academic Publishers, 2004
[2] A. M. Niknejad, R. G. Meyer, "Design, Simulation and Applications of Inductors and Transformers for SI RF ICS", Kluwer Academic Publishers, 2002
[3] R. Thüringer, "Characterization of Integrated Lumped Inductors and Transformers", Wien, April, 2002
[4] XFAB, "0,35 µm Process Family, XU035"
[5] H. M. Greenhouse, "Design of planar rectangular microelectronic inductors", IEEE Transaction on Parts, Hybrids, and Packaging, Vol. PHP-10, No. 2, June 1974